depositing a silicon cap layer over said first forming silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon.

26. A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal containing silicon or an alloy thereof on a bulk silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy; and

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second phase; and

etching any unreacted silicon, wherein said metal is nickel.

REMARKS

An Excess Claim Fee Payment Letter for an excess independent claim is being filed concurrently herewith.

Claims 1-13 and 23-26 are all of the claims pending. Claim 9 and non-elected claims 14-22 have been canceled. New claims 23-26 have been added to more completely define the invention.

Applicant gratefully acknowledges the Examiner's indication that claims 10-11 would be allowable if rewritten in independent form. Claim 10 has been rewritten accordingly to place

these claims into condition for immediate allowance.

Claims 1-8 and 12-13 stand rejected on prior art grounds. Claims 5 and 9 stand rejected under 35 U.S.C. §112, first paragraph, and claims 8 and 9 stand rejected under 35 U.S.C. §112, second paragraph.

With regard to the prior art rejections, claims 1-2, 4-5, 8 and 12-13 stand rejected under 35 U.S.C. §102 (e) as being anticipated by Besser et al.(U.S. Patent No. 6,165,903), claims 1-, 3, and 13 stand 35 rejected under 35 U.S.C. §102 (e) as being anticipated by Kanamori (U.S. Published Patent Application No. 09/398,189), and claims 2, 4-8, and 12 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Kanamori in view of Besser.

These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the claims and specification by the current Amendment.

It is noted that the claim amendments herein are made only for more particularly pointing out the invention for the Examiner, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., see independent claim 1), is directed to a method for fabricating a silicide for a semiconductor device, which includes depositing a metal containing silicon or an alloy thereof on a silicon substrate, reacting the metal containing silicon or the alloy to form a first silicide phase, etching any unreacted metal

containing silicon, depositing a silicon cap layer over the first silicide phase, reacting the silicon cap layer to form a second silicide phase, for the semiconductor device, and etching any unreacted silicon.

Independent claims 4 and 13 recite somewhat similar methods, but with some different limitations.

With such features, a reaction of metal (e.g., Co in an exemplary embodiment, but other metals will be similarly operable as claimed and as clearly described int eh specification) to initially form Co_2Si, minimizes the silicon consumption of the thin SOI film (or bulk silicon) substrate. The consumption of the thin SOI film is additionally reduced by the deposition of a silicon or poly-silicon film on the Co_2Si.

The present invention extends the use of a salicide-like process to thin SOI films, which are expected to be used in future SOI MOSFETs. Such thin-film SOI films will be advantageous in making the devices smaller, reducing the source/drain to substrate overlap capacitance, and eliminating the floating body voltage.

Further, with the invention, it is further possible to obtain good control in forming a silicide over the source and drain in bulk crystalline silicon structures as well as thin film SOI structures.

Such features are not taught or suggested by any other prior art of record, either alone or in combination.

II. THE 35 U.S.C. §112, FIRST PARAGRAPH, REJECTION

Applicant submits that the specification is clearly enabling for not only Co and Ti, but also for Ni. That is, one of ordinary skill in the art would be able to make and use the invention without undue experimentation.

However, to clarify the invention for the Examiner, claims 5 and 9 have been amended.

Further, as is known, it is noted that silicides have many different phases. Along these lines, using nickel is indeed possible and NiSi phase is a preferred structure and offers lower resistivity phase (e.g., as compared to $NiSi_2$). In the case of Nickel, it is possible to form the first forming phases, which is not necessarily NiSi, and the cap can be used in forming these phases as well as the NiSi phase.

Hence, the invention can use the silicon cap advantageously in going from one phase to another, and not necessarily to be used for all phases. Hence, unlike cobalt where it may be advantageous to go all the way through the phases (e.g., $CoSi_2$), it may be advantageous to stop the process at NiSi in the case of nickel. That is, the silicon cap can be advantageously used between phases, including prior to NiSi. Hence, the two phases could be Ni_2Si and NiSi. By the same token, in the case of Nickel it is more complicated (as compared to cobalt, etc.) since realistically there are several other phases before NiSi. Thus, the inventive method is advantageous even if not all of the phases possible are passed through.

Further, independent claim 26 has been added and is directed to the Ni application of the invention.

In view of the foregoing, reconsideration and withdrawal of this rejection are respectfully requested.

III. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

While Applicant submits that the claims are clear to one of ordinary skill in the art to recognize the metes and bounds of the invention, to speed prosecution, claims 8 and 9 have been amended in a manner believed fully responsive to the Examiner's criticisms.

Reconsideration and withdrawal of this rejection are respectfully requested.

IV. THE PRIOR ART REJECTIONS

A. The Rejections based on Besser et al. and/or Kanamori References

Besser et al. discloses a method of forming ultra-shallow junctions in a semiconductor wafer with deposited silicon layer to reduce silicon consumption during salicidation.

Further, Kanamori discloses a method of fabricating a semiconductor device self-aligned silicide areas formed using a supplemental silicon overlayer. Such methods are completely and fundamentally different from that of the invention.

Specifically, the claimed invention is clearly distinguished from Besser and Kanamori by the use of an alloy (e.g., Co_xSi_{1-x}) or a metal containing silicon (e.g., a metal-silicon mixture), rather than a pure metal. The use of the alloy encapsulates two important advantages of the claimed invention, which are not shared by Besser and/or Kanamori.

First, the alloy or metal-silicon mixture already contains some of the silicon required to form the silicide. Thus, less silicon is consumed from the substrate during the subsequent anneal. Indeed, none of the references teaches or suggests using such a metal-silicon mixture, let alone for the reason and purpose of the invention.

Secondly, as clearly defined by new claim 25, using an alloy enables applying the silicon cap to the very first forming phase (e.g., Co_2Si), rather than a later phase (e.g., CoSi) as allegedly taught by Besser and Kanamori.

Indeed, the known metal (e.g., cobalt will be employed in this exemplary embodiment) silicide phases in the order that they form are illustrated in Figure 1 of the Exhibit attached hereto. The resistivity and formation temperature of each phase are also indicated. By applying the silicon cap to the Co_2Si phase, silicon is supplied from the cap already during the reaction that forms the CoSi phase. The silicon consumption from the substrate is then reduced during the formation of the CoSi and the $CoSi_2$ phase, which is a significant improvement over the methods of Besser and/or Kanamori.

Furthermore, it is noted that the use of the metal-silicon mixture is fundamental to the inventive method and would not have been obvious to Besser or Kanamori. This can be better shown referring to the diffraction maps shown in Figure 2 of the attached Exhibit.

The top map (e.g., Figure 1) shows the evolution of the Co-silicide phases when pure Co metal is used (as opposed to a metal containing silicon or an alloy, as in the claimed invention).

At a temperature lower than about 440C, no reaction takes place, and only pure Co is measured. Then, when the temperature is increased, the Co_2Si phase forms and exists only within a narrow window of about 20C, after which the phase changes into CoSi.

The CoSi phase persists up to 625C where it changes into $CoSi_2$. Since the Co_2Si phase only exists in a very narrow, tight temperature window, it is very difficult to form (e.g., very unreliable and prone to error or being missed based on nonuniform doping of the substrate, etc.),

and, in practice, the later phase (e.g., CoSi) is used in self-aligned silicide processes.

The bottom map (e.g., Figure 2) shows the evolution of reacting a metal (e.g., Co) containing silicon or an alloy, as in the claimed invention.

That is, Figure 2 shows the metal (e.g., Co)-silicide phases when a Co-silicon mixture having 20% silicon is used instead of pure Co. In this case, the Co_2Si phase exists over a large temperature window of more than 100C. This makes it possible to practice a self-aligned silicide process where the first phase is also the first forming phase (Co_2Si). As a result, much more reliable and easier manufacturing processes are possible since it is easier to stop on Co_2Si, etc. Then, annealing can be performed, etc. to go to CoSi, and finally to $CoSi_2$. Again, Applicant submits that such is not trivial to use the method above (including using the metal-silicon mixture or an alloy) as described above, as one must provide a method of using it. The references have provided no such method for using it. Thus, it would not have been obvious to one of ordinary skill in the art taking Besser and/or Kanamori. Indeed, using CoSi would not have been obvious, and no method has been provided therefor by any of the references.

Thus, using the metal containing silicon or an alloy, as in the invention, produces unexpectedly superior results, as clearly shown in a comparison of the Figures in Exhibit 1. Again, in the invention, including some of the silicon in the metal is better than what Besser is doing since less silicon is consumed in the inventive method. That is, some of the silicon is being provided by the metal-silicon mixture or alloy.

Further (and maybe more importantly), using the metal-silicon mixture or alloy does not simply allow more silicon to be provided, but it allows the invention can stop on the first silicide

forming phase (e.g., Co_2Si) because a wider temperature window is being provided. Again, the inventors have recognized that providing the silicon cap as early as possible in the process, is advantageous.

That is, if the silicon cap is provided when the phase is, for example, Co_2Si, then another source of silicon is provided, thereby reducing (e.g., halving) the amount of silicon needed from the substrate or the like in the next phase (e.g., CoSi).

Besser, at most, starts to obtain the benefit of applying the silicon cap (if any) only at the very last phase (e.g., forming of the $CoSi_2$ phase), not the very first forming silicide phase as in new claim 25. Again, the invention applies the cap much earlier, and hence, the invention obtains the benefit of the cap much earlier.

In sum, the invention applies and reacts the metal containing silicon or an alloy to form a first silicide phase. Indeed, Besser and Kanamori do not even address the forming of phases.

Further, there is no teaching or suggesting of reacting a metal or alloy to form the first forming silicide phase, as defined by independent claim 25. That is, the invention wants to react the metal or alloy in the phase which is first formed. The inventors have recognized that, as the reaction continues, more and more silicon is consumed. Thus, the invention recognizes that performing the reacting to form the phase which consumes as little silicon as possible is the most desirable. Hence, the invention of independent claim 25 reacts the metal or the alloy in the very first phase which is formed. However, none of the references has even recognized the advantages of even performing such an operation.

Further, Applicant notes that the Examiner in his reference to the allowability of claims

10-11 acknowledges that Besser and Kanamori do not teach the use of alloys or metal-silicon mixture.

Moreover, both Besser and Kanamori are mute about the lowest consumption phase, Co_2Si, and only discuss the high resistivity phase CoSi as the first silicide phase to be used in their processes. CoSi is not the first forming phase and thus is clearly distinguished from the claimed invention. Hence, the invention is not rendered obvious by any of Besser and Kanamori.

Thus, turning to the claim language, there is no teaching or suggestion of "*[a] method for fabricating a silicide for a semiconductor device, said method comprising:*

depositing a metal containing silicon or an alloy thereof on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon" (emphasis Applicant's), as defined by independent claim 1, and somewhat similarly in independent claims 4 and 13.

Further, there is no teaching or suggestion of new claim 25 which recites "*[a] method for fabricating a silicide for a semiconductor device, said method comprising:*

depositing a metal or an alloy thereof on a silicon substrate;

reacting said metal or said alloy to form a first forming silicide phase;

etching any unreacted metal or alloy;

depositing a silicon cap layer over said first forming silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon (emphasis Applicant's).

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Besser et al. and Kanamori fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

Applicant has submitted all references believed to be relevant to the claimed invention under 37 C.F.R. §1.56 and §§1.97-1.99, and is aware of its continuing duty of disclosure.

In response to the Examiner's objection to the drawings, Applicant points out that Figures 1, 7A, 7B, and 8 are described as "conventional" and as "related art" as opposed to "prior art" usable against the present invention. Such Figures were not necessarily published outside the confines of IBM Corporation, and thus to label these Figures as "Prior Art" at this time would be erroneous.

To overcome the Examiner's Rule 84(p)(5) objection, submitted herewith is a Submission of Proposed Drawings Corrections to Figures 1-6 to label them with the reference numerals.

With regard to the Examiner's Rule 83 objection to the drawing, Applicant submits that

all claimed subject matter is in fact shown in the drawings. The bulk silicon is shown schematically in the drawings. Further, the TiN or W cap has been shown with reference numeral 21. No new matter has been added.

The specification has been amended to overcome the Examiner's objection to the disclosure.

In view of the foregoing, Applicant submits that claims 1-14 and 23-26, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 5/14/02

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VERSION SHOWING MARKINGS MADE

IN THE SPECIFICATION:

Please replace the paragraph on page 11, line 6 with the following paragraph:

Figures 9A and 9B illustrate the novelty [fo] of the inventive structure.

Please replace the paragraph on page 12, line 6 with the following paragraph:

Referring to Figure 2, a metal 20 (e.g., Co, Ni, Ti, Pd, Pt or alloys thereof) is deposited in a thickness within a range of about 7-8 nm. A TiN cap or a W cap [(not shown in the Figure)] 21 is deposited over the metal 20 to prevent oxidation during the anneal. The metal 20 is reacted with silicon in the source 4, drain 5, and gate 7 regions at a low temperature T_1. It is noted that if the temperature is too low, no reaction will take place. On the other hand, if the temperature is too high, then the monosilicide phase of CoSi will be formed. Since the temperature window over which the metal-rich phase Co_2Si is formed is narrow, it is difficult to achieve only this phase during the first anneal. To extend the temperature window, a mixture of 80% Co and 20% Si may be deposited (e.g., by co-sputtering or evaporation from a $Si_{0.2}Co_{0.8}$ target). The temperature window for the formation of the Co_2Si out of the $Si_{0.2}Co_{0.8}$ mixture is about 337°C to about 487°C. The use of a 80% Si and 20% Co to extend the temperature window is described

in U.S. Patent [Application] No. [09/515,033] 6,323,130, to Cyril Cabral et. al, entitled "METHOD FOR SELF-ALIGNED FORMATION OF SILICIDE CONTACTS USING METAL SILICON ALLOYS FOR LIMITED SILICON CONSUMPTION AND FOR REDUCTION OF BRIDGING", filed on March 6, 2000[, having IBM Docket No. YOR900-0044], incorporated herein by reference.

Please replace the paragraph on page 18, line 3 with the following paragraph:

The silicon consumption may be further reduced if a mixture of Co and Si is deposited in the first step above. The process of using Co alloys was first disclosed in the above-mentioned U.S. Patent No. 6,323,130 [copending application Serial No. 09/515,033]. Thus, instead of a pure Co deposition (step 1), Co is co-deposited with Si. The use of such a mixture of $Co_{1-x}Si_x$, is limited to about $x<0.3$, or otherwise bridging from source/drain to gate would occur. The reduction in the Si consumption from the wafer is achieved due to the following reasons:

IN THE CLAIMS:

Please cancel claims 9 and 14-22 without prejudice or disclaimer.

1. (Amended) A method for fabricating a silicide for a semiconductor device, said method comprising:

depositing a metal containing silicon or an alloy thereof on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon.

4. (Amended) A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal containing silicon or an alloy thereof on a bulk silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase; and

etching any unreacted silicon.

5. (Amended) The method of claim 4, wherein said depositing of said metal containing silicon comprises performing a blanket deposition of a metal comprising one of Co[,] and Ti [and Ni].

8. (Amended) The method of claim 4, [further comprising:]

wherein said reacting of said metal comprises performing a first rapid thermal anneal

(RTA) to form a metal-silicon phase, such that the deposited metal containing silicon with the underlay Si, converts some of the Si into metal-Si[;],

wherein said etching comprises selectively etching any unreacted metal, thereby leaving the metal-silicon regions intact[;],

wherein said depositing comprises performing a blanket deposition of a silicon film[;], and

wherein said reacting of said silicon cap comprises performing a second RTA to form a metal di-silicide.

10. (Amended) A method for fabricating a silicide for a silicon region, said method comprising:

depositing a metal or an alloy thereof on a bulk silicon substrate;

reacting said metal or said alloy to form a first silicide phase;

etching any unreacted metal or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase; and

etching any unreacted silicon,

[The method of claim 4,] wherein said metal is co-deposited with silicon.

13. (Amended) A method for fabricating a silicide, said method comprising:

providing a substrate having a silicon layer;

depositing a metal containing silicon or an alloy over said silicon layer;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy; and

depositing a silicon cap layer over said metal containing silicon or said alloy;

reacting the silicon cap layer, to form a second silicide phase; and

etching any unreacted silicon.

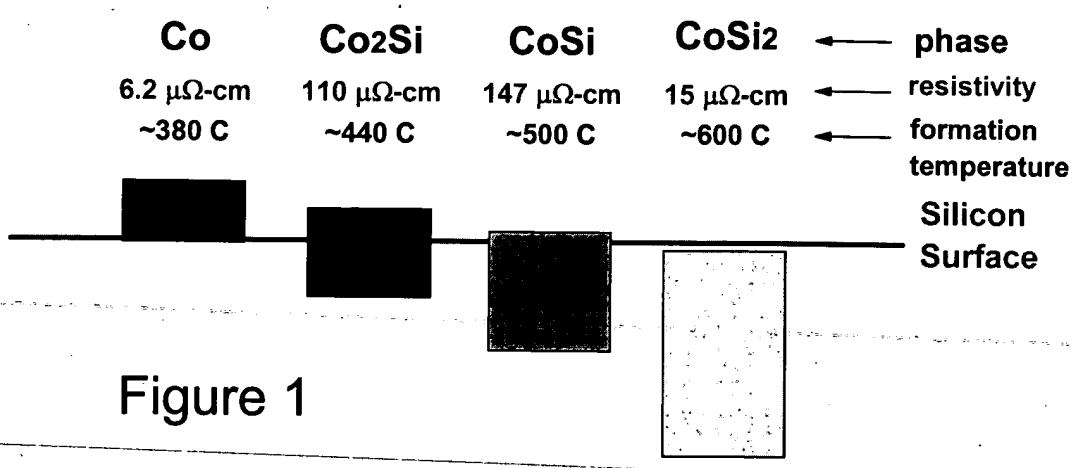

Figure 1

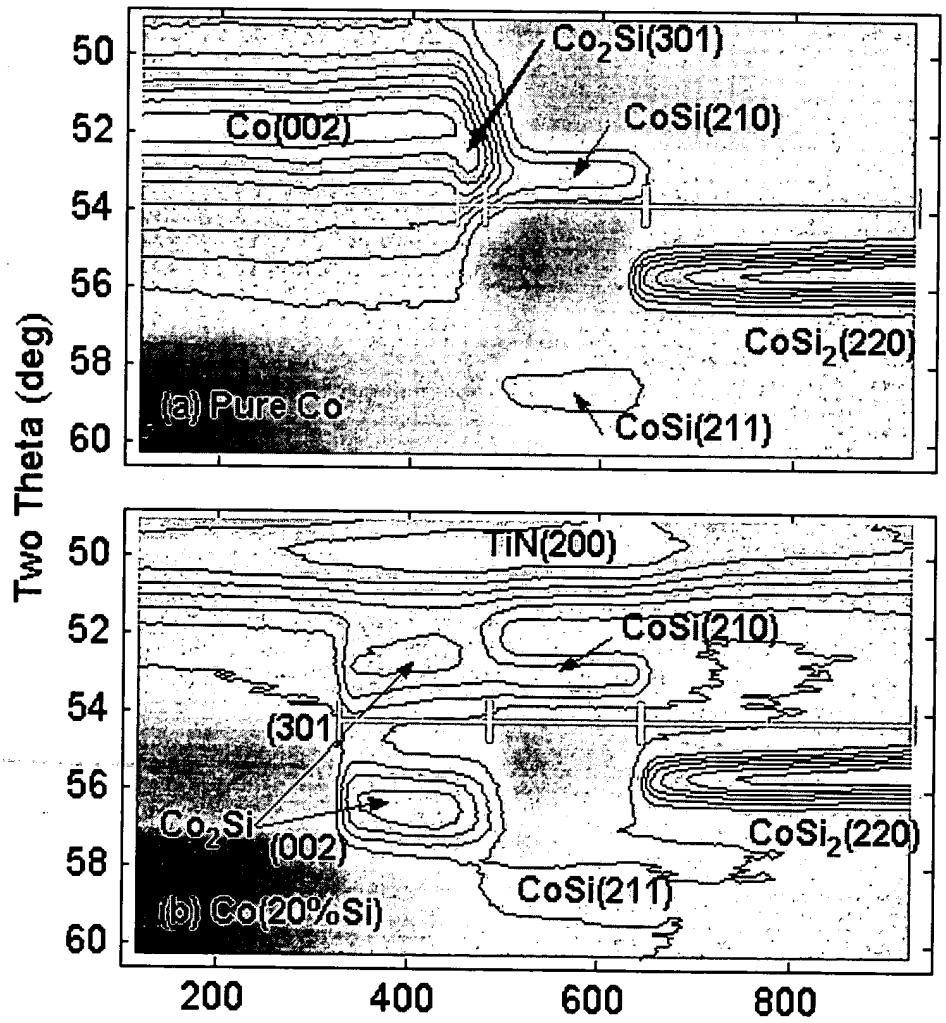

figure 2

Exhibit I